CLAIMS

What is claimed is:

1. A method for fabricating a gate electrode, wherein said method comprising:

providing a substrate;

forming a first barrier layer on said substrate;

forming a dielectric layer with a high dielectric constant on said first barrier layer;

forming a metal gate layer on said dielectric layer; and

removing a portion of said metal gate layer, said dielectric layer, and said first barrier layer to form a gate electrode on said substrate.

2. The method according to claim 1, wherein the steps of forming said first barrier layer comprises a first nitrogen-containing rapid thermal process.

3. The method according to claim 2, wherein said first nitrogen-containing rapid thermal process further comprising an ammonia rapid thermal process.

4. The method according to claim 2, wherein the temperature of said first nitrogen-containing rapid thermal process is between 600

℃ to 750 ℃.

5. The method according to claim 2, wherein the duration of said first nitrogen-containing rapid thermal process is between the 10 to 20 minutes.

6. The method according to claim 1, wherein material of said first barrier layer is selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (SiN_x), and silicon oxynitride (SiON).

7. The method according to claim 1, wherein material of said dielectric layer is selected from the group consisting of zirconium dioxide (ZrO_2), hafnium dioxide (HfO_2), zirconium silicates (Zr-silicates), hafnium silicates (Hf-silicates), La_2O_3 (lanthanum oxide), Y_2O_3 (yttrium oxide), and Al-doped Zr-silicate ($(Al_2O_3)(ZrO_2)_x(SiO_2)_{1-x-y}$).

8. The method according to claim 1, wherein said dielectric layer with said high dielectric constant is about 10.

9. The method according to claim 1, wherein the steps of said fabricating said gate electrode on said substrate further comprising:

performing a post-deposition annealing to said dielectric layer;

depositing a second barrier layer on said dielectric layer;

depositing a metal gate layer on said second barrier layer;

forming a photoresist layer on said metal gate layer; and

sequentially etching said metal gate layer, said second barrier layer, said dielectric layer, and said first barrier layer to form a gate electrode on said substrate.

10. The method according to claim 9, wherein the temperature of said post-deposition annealing is between 700 ℃ to 900 ℃.

11. The method according to claim 9, wherein the duration of said post-deposition annealing is between 20 to 45 minutes.

12. The method according to claim 9, wherein the material of said second barrier layer is selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (SiN_x), and silicon oxynitride (SiON).

13. The method according to claim 9, further comprising a second nitrogen-containing rapid thermal process treatment on said gate electrode.

14. The method according to claim 9, wherein said second nitrogen-containing rapid thermal process comprises an ammonia rapid thermal process.

15. The method according to claim 9, wherein the material of said metal gate layer is selected from the group consisting of tantalum (Ta), tantalum nitride (TaN_x), and $TaRu_xN_y$ (tantalum-ruthenium-nitrogen).

16. A method for fabricating a gate electrode, said method comprising:

providing a substrate;

treating said substrate by a first nitrogen-containing rapid thermal process to form a first barrier layer thereon;

depositing a dielectric layer with a high dielectric constant on said first barrier layer;

performing a post-deposition annealing process on said dielectric layer;

forming a second barrier layer on said dielectric layer;

forming a metal gate layer on said second barrier layer;

forming a photoresist layer on said metal gate layer;

sequentially etching said metal gate layer, said second barrier layer, said dielectric layer, and said first barrier layer to form a gate electrode on said substrate; and

performing a second nitrogen-containing rapid thermal process on said gate electrode.

17. The method according to claim 16 wherein said first

nitrogen-containing rapid thermal process further comprising an ammonia rapid thermal process.

18. The method according to claim 16, wherein the temperature of said first ammonia rapid thermal process (NH_3 RTP) is between 600 ℃ to 750 ℃.

19. The method according to claim 16, wherein the duration of said first nitrogen-containing rapid thermal process is between the 10 to 20 minutes.

20. The method according to claim 16, wherein material of said first barrier layer is selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (SiN_x), and SiON (silicon oxynitride).

21. The method according to claim 16, wherein said dielectric layer is selected from the group consisting of zirconium dioxide (ZrO_2), hafnium dioxide (HfO_2), zirconium silicates (Zr-silicates), hafnium silicates (Hf-silicates, La_2O_3 (lanthanum oxide), Y_2O_3 (yttrium oxide), and Al-doped Zr-silicate ($(Al_2O_3)(ZrO_2)_x(SiO_2)_{1-x-y}$).

22. The method according to claim 16, wherein said dielectric layer with said high dielectric constant is about 10.

23. The method according to claim 16, wherein said performing post-deposition annealing comprises a post-deposition annealing in nitrogen gas.

24. The method according to claim 23, wherein the temperature of said post-deposition annealing is between 700 ℃ to 900 ℃.

25. The method according to claim 23, wherein the duration of said post-deposition annealing is between 20 to 45 minutes.

26. The method according to claim 16, wherein the material of said second barrier layer is selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (SiN_x), and SiON (silicon oxynitride).

27. The method according to claim 16, wherein the material of said metal gate layer is selected from the group consisting of tantalum (Ta), tantalum nitride (TaN_x), and $TaRu_xN_y$ (tantalum-ruthenium-nitrogen).

28. The method according to claim 16, wherein said second nitrogen-containing rapid thermal process further comprising an ammonia rapid thermal process.

29. A method for forming the gate electrode, said method comprising:

providing a substrate;

treating said substrate by a first ammonia rapid thermal process (NH_3 RTP) to form a first barrier layer on said substrate;

chemical vapor depositing a dielectric layer on said first barrier layer, wherein the dielectric constant of said dielectric layer is about 10;

performing a post-deposition annealing in nitrogen gas on said dielectric layer;

chemical vapor depositing a second barrier layer on said dielectric layer;

chemical vapor depositing a metal gate layer on said second barrier layer;

forming a photoresist layer on said metal gate layer;

sequentially etching said metal gate layer, said second barrier layer, said dielectric layer, and said first barrier layer to form a gate electrode on said substrate; and

performing a second ammonia rapid thermal process (NH_3 RTP) on said gate electrode to form a surface inhibition layer on the sidewall of said gate electrode.

30. The method according to claim 29, wherein the

temperature of said first ammonia rapid thermal process (NH_3 RTP) is between 600 ℃ to 750 ℃.

31. The method according to claim 29, wherein the duration of said first ammonia rapid thermal process (NH_3 RTP) is between 10 to 20 minutes.

32. The method according to claim 29, wherein material of said first barrier layer is selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (SiN_x), and silicon oxynitride (SiON).

33. The method according to claim 29, wherein said dielectric layer is selected from the group consisting of zirconium dioxide (ZrO_2), hafnium dioxide (HfO_2), zirconium silicates (Zr-silicates), and hafnium silicates (Hf-silicates), and La_2O_3 (lanthanum oxide), Y_2O_3 (yttrium oxide), and Al-doped Zr-silicate ($(Al_2O_3)(ZrO_2)_x(SiO_2)_{1-x-y}$).

34. The method according to claim 29, wherein the temperature of said post-deposition annealing is between 700 ℃ to 900 ℃.

35. The method according to claim 29, wherein the duration of said post-deposition annealing is between 20 to 45 minutes.

36. The method according to claim 29, wherein the material of said second barrier layer is selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (SiN_x), and SiON (silicon oxynitride).

37. The method according to claim 29, wherein the temperature of said second ammonia rapid thermal process is about 600 ℃.

38. The method according to claim 29, wherein the duration of said second ammonia rapid thermal process is about 20 minutes.

39. The method according to claim 29, wherein said surface inhibition layer comprises TaN_x.